Detailed: (changes in red and deleted one is marked as ~~deleted~~)

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| **sSvs4a** | **Subscribe SV with simulation parameter set – preferred variant** | **[ ]  Passed****[ ]  Failed****[ ]  Inconclusive** |
| IEC 61869-9PIXIT Svs1a, Svs1b, Svs3 |
| Expected result1. DUT subscribes ~~the real sampled values~~ SV1 ~~according to PIXIT~~, LSVS.St = TRUE, LSVS.SimSt=FALSE2. DUT ignores the simulated sampled values SV2, LSVS.St = TRUE, LSVS.SimSt=FALSE3. DUT indicates loss of SV stream ~~according to PIXIT~~, LSVS.St changes to FALSE (LSVS.SimSt = FALSE)4. DUT subscribes ~~the real sampled values~~ SV1 and SV3 according to PIXIT, LSVS.St = TRUE, LSVS.SimSt=FALSE5. DUT subscribes to the simulated SV2 stream according to PIXIT LSVS.SimSt changes to TRUE and  DUT subscribes to the real SV3 stream ~~according to PIXIT~~, no change in LSVS 6. DUT indicates loss of SV2 stream ~~according to PIXIT~~, LSVS.St changes to FALSE7. DUT subscribes the ~~real sampled values~~ SV1 according to PIXIT, LSVS.St = TRUE, LSVS.SimSt=FALSE |
| Test descriptionConfigure the DUT to subscribe to the maximum preferred variant of all preferred variants, and the lowest rate backwards compatible stream. Below, SV1 and SV2 send same maximum preferred variant SV streams differing only in Simulation bits. SV3 sends backwards compatible SV stream without simulation bit sets. SV1 and SV2 are supervised by LGOS1, SV3 is supervised by LGOS2.Test engineer forces LPHD.Sim=False or LPHD.Sim is absent 1. SIMULATOR publishes SV1 stream with the simulation bit not set2. SIMULATOR publishes ~~one~~ SV2 stream with the simulation bit set with new current/voltage values and ~~another~~ SV1 stream with the simulation bit not set3. SIMULATOR publishes only SV2 stream with the simulation bit setWhen LPHD.Sim is present, test engineer forces LPHD.Sim=True and perform steps 4-7: 4. SIMULATOR publishes ~~two~~ ~~real~~ SV1 and SV3 stream with the simulation bit not set and continues publishing during step 5 and 65. SIMULATOR adds ~~a third simulated~~ SV2 stream with the simulation bit set with new current/voltage values6. SIMULATOR stops ~~the third simulated~~ SV2 stream with the simulation bit setTest engineer forces LPHD.Sim=False 7. SIMULATOR publishes simulated SV2 stream with the simulation bit set and the real SV1 stream with the simulation bit not set |
| CommentNote: LSVS is optional and only verified when available. When LSVS is available the LSVS.SimSt is optionalTested with configuration: X |

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| **sSvs4a** | **Subscribe SV with simulation parameter set – backward compatible variant** | **[ ]  Passed****[ ]  Failed****[ ]  Inconclusive** |
| IEC 61869-9PIXIT Svs1a, Svs1b, Svs3 |
| Expected result1. DUT subscribes ~~the real sampled values~~ SV3 according to PIXIT, LSVS.St = TRUE, LSVS.SimSt=FALSE2. DUT ignores the simulated sampled values SV4, LSVS.St = TRUE, LSVS.SimSt=FALSE3. DUT indicates loss of SV stream according to PIXIT, LSVS.St changes to FALSE (LSVS.SimSt = FALSE). 4. DUT subscribes ~~the real sampled values~~ SV1 and SV3 according to PIXIT, LSVS.St = TRUE, LSVS.SimSt=FALSE5. DUT subscribes to the simulated SV4 stream ~~according to PIXIT~~ LSVS.SimSt changes to TRUE and  DUT subscribes to the real SV3 stream ~~according to PIXIT~~, no change in LSVS 6. DUT indicates loss of SV4 stream according to PIXIT, LSVS.St changes to FALSE7. DUT subscribes the ~~real sampled values~~ SV3 ~~according to PIXIT~~, LSVS.St = TRUE, LSVS.SimSt=FALSE |
| Test descriptionConfigure the DUT to subscribe to the maximum preferred variant of all preferred variants, and the lowest rate backwards compatible stream. Below, SV3 and SV4 send same backwards compatible streams differing only in Simulation bits.SV1 send maximum preferred variant SV streams differing without simulation bit sets. SV1 is supervised by LGOS1, SV3 and SV4 is supervised by LGOS2.Test engineer forces LPHD.Sim=False or LPHD.Sim is absent 1. SIMULATOR publishes SV3 stream with the simulation bit not set2. SIMULATOR publishes ~~one~~ SV4 stream with the simulation bit set with new current/voltage values and ~~another~~ SV3 stream with the simulation bit not set3. SIMULATOR publishes only SV3 stream with the simulation bit setWhen LPHD.Sim is present, test engineer forces LPHD.Sim=True and perform steps 4-7: 4. SIMULATOR publishes ~~two~~ ~~real~~ SV1 and SV3 stream with the simulation bit not set and continues publishing during step 5 and 65. SIMULATOR adds ~~a third simulated~~ SV4 stream with the simulation bit set with different current/voltage values6. SIMULATOR stops ~~the third simulated~~ SV4 stream with the simulation bit setTest engineer forces LPHD.Sim=False 7. SIMULATOR publishes simulated SV3 stream with the simulation bit set and the real SV1 stream with the simulation bit not set |
| CommentNote: LSVS is optional and only verified when available. When LSVS is available the LSVS.SimSt is optionalTested with configuration: XThis test case is only applicable when PIXIT entry Svs3 is marked as Y for backwards compatible rates.  |

Also the PIXIT entry Svs3 shall be updated

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| Svs3 | Support simulation mode* Preferred rates
* Backwards compatible rates

How to enable simulation mode | YY/NLPHD.Sim or describe |