Solution to redmine 6210

Svs4 misses the test for backwards compatable rate

February 21, 2023

PIXIT Entry Svs3 is wrong. There shall not be difference for preferred of backward rate with regard to simulation.  
Either is simulation supported or not.  
In other word both Y or both N.  
Additionally, how can simulation be enabled without LPHD.Sim? This only be can done and tested with the usage of LPHD.Sim.  
Propose to deprecate Svs3.

sSvs4 should not consider other approach for simulation than using LPHD.Sim.  
sSvs4 Expected result do not need to consider the Svs3 PIXIT entry.

Solution: remove pixit entry from sSvs4

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| **sSvs4** | **Subscribe SV with simulation parameter set** | **Passed**  **Failed**  **Inconclusive** |
| IEC 61869-9  PIXIT Svs1a, Svs1b, ~~Svs3~~ | | |
| Expected result  1. DUT subscribes the real sampled values according to PIXIT, LSVS.St = TRUE, LSVS.SimSt=FALSE  2. DUT ignores the simulated sampled values, LSVS.St = TRUE, LSVS.SimSt=FALSE  3. DUT indicates loss of SV stream according to PIXIT, LSVS.St changes to FALSE (LSVS.SimSt = FALSE)  4. DUT subscribes the real sampled values according to PIXIT, LSVS.St = TRUE, LSVS.SimSt=FALSE  5. DUT subscribes to the simulated SV1 stream according to PIXIT LSVS.SimSt changes to TRUE and  DUT subscribes to the real SV2 stream according to PIXIT, no change in LSVS  6. DUT indicates loss of SV1 stream according to PIXIT, LSVS.St changes to FALSE  7. DUT subscribes the real sampled values according to PIXIT, LSVS.St = TRUE, LSVS.SimSt=FALSE | | |
| Test description  Configure the DUT to subscribe to the maximum preferred variant of all preferred variants  Test engineer forces LPHD.Sim=False or LPHD.Sim is absent  1. SIMULATOR publishes SV stream with the simulation bit not set  2. SIMULATOR publishes one SV stream with the simulation bit set and another SV stream with the simulation bit not set  3. SIMULATOR publishes only SV stream with the simulation bit set  When LPHD.Sim is present, test engineer forces LPHD.Sim=True and perform steps 4-7:  4. SIMULATOR publishes two real SV1 and SV2 stream with the simulation bit not set and continues publishing during step 5 and 6  5. SIMULATOR adds a third simulated SV1 stream with the simulation bit set  6. SIMULATOR stops the third simulated SV1 stream with the simulation bit set  Test engineer forces LPHD.Sim=False  7. SIMULATOR publishes simulated SV1 stream with the simulation bit set and the real SV1 stream with the simulation bit not set | | |
| Comment  Note: LSVS is optional and only verified when available. When LSVS is available the LSVS.SimSt is optional  Tested with configuration: X | | |

PIXIT Svs3; not required anymore; when LPHD.Sim is present in the datamodel simulation is supported

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| Svs3 | <depricated> |  |